

FIG. 1

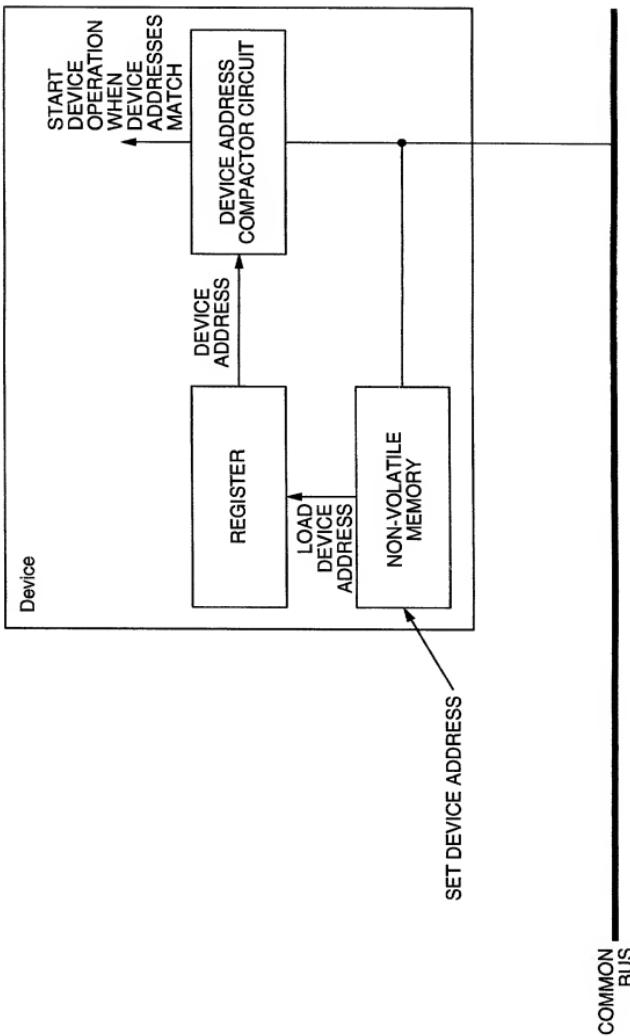


FIG. 2

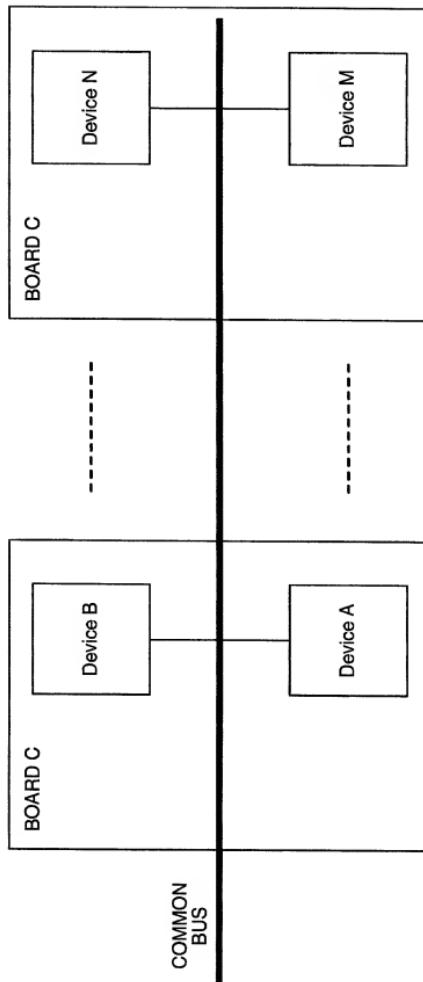


FIG. 3

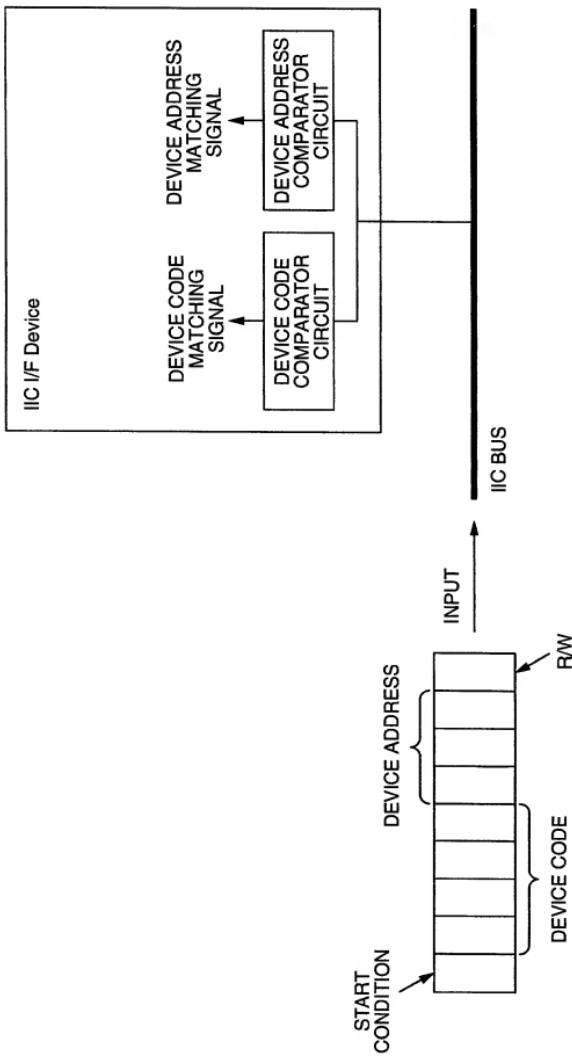


FIG. 4

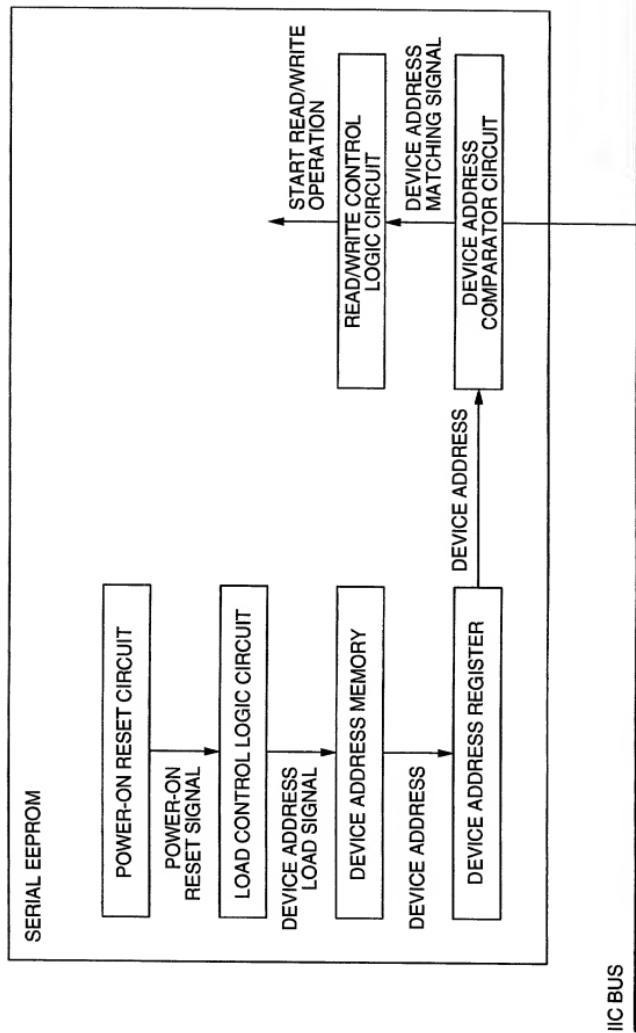


FIG. 5

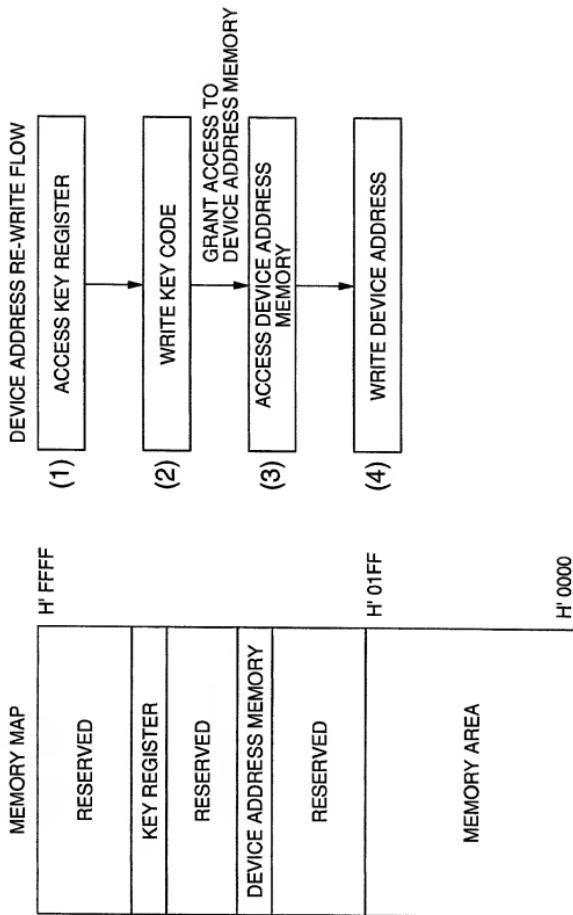


FIG. 6

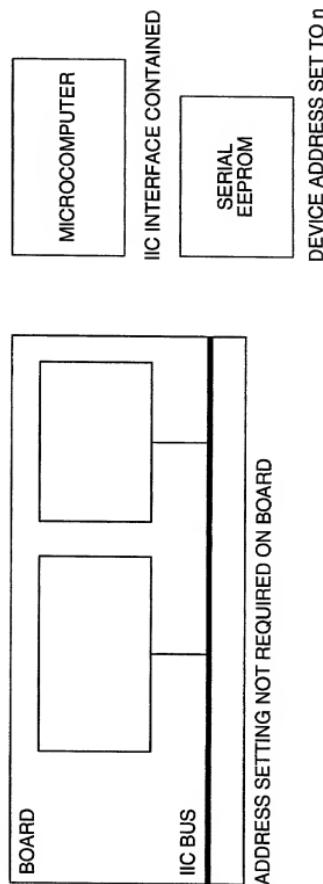
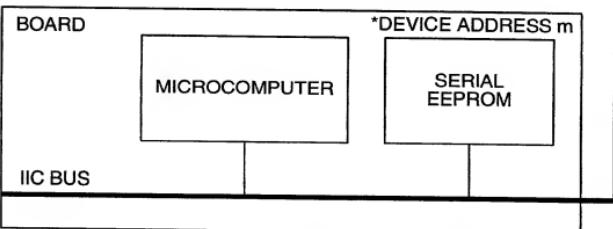
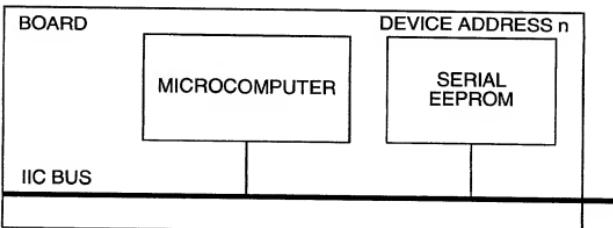
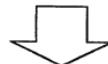
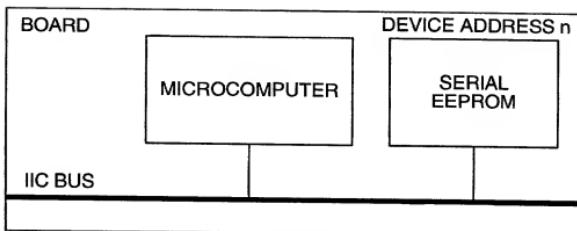


FIG. 7

EEPROM-EQUIPPED MICROCOMPUTER SYSTEM (2 CPUS)
OPERABLE AS SERIAL EEPROMS HAVING ADDRESSES n,m

FIG. 8

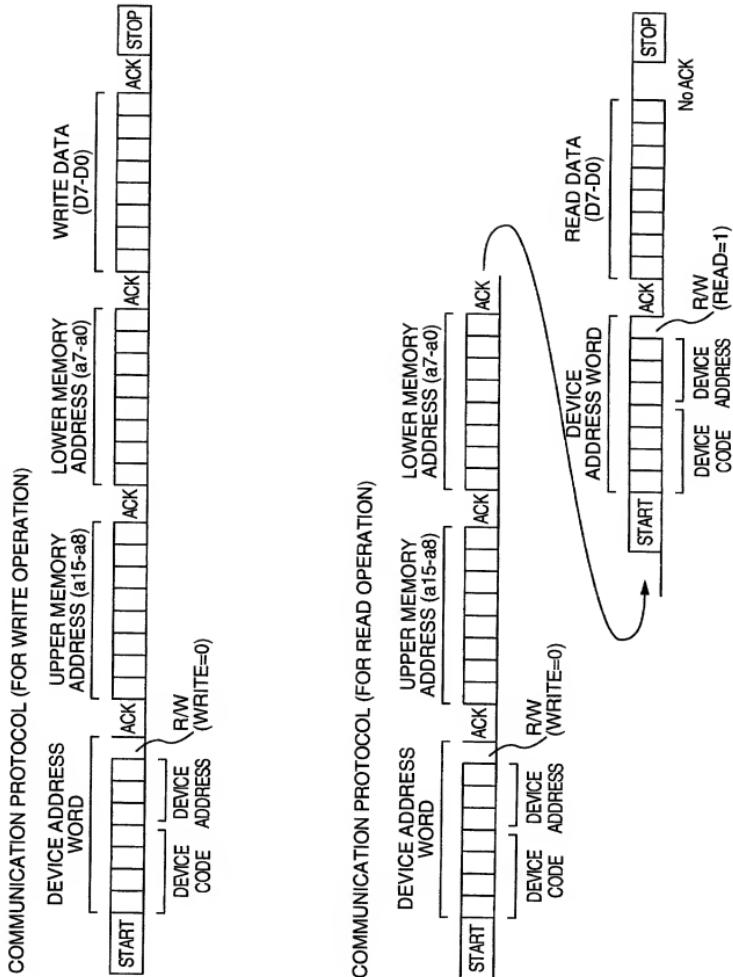
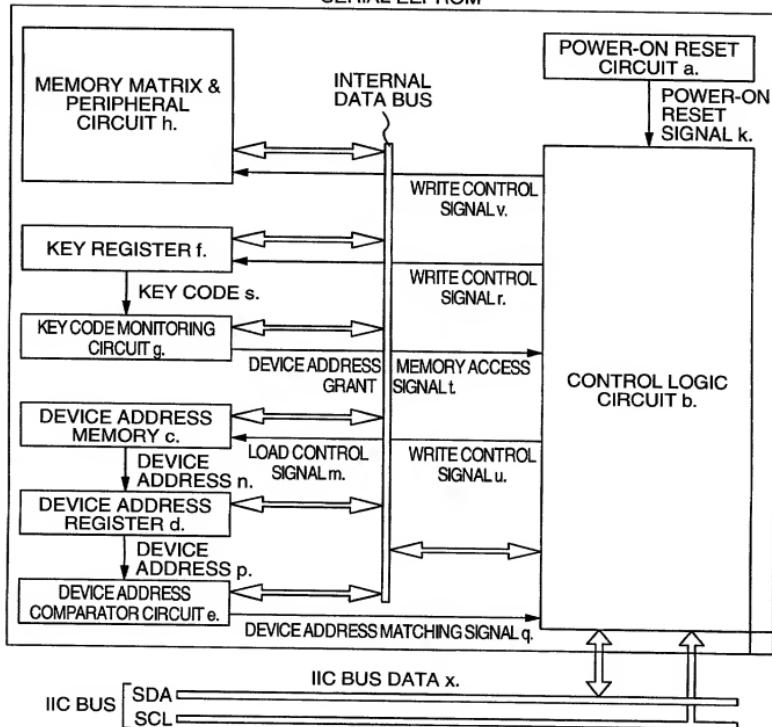


FIG. 9

SERIAL EEPROM



IIC BUS DATA x.	DEVICE ADDRESS WORD*	UPPER MEMORY ADDRESS	LOWER MEMORY ADDRESS	WRITE DATA
1	10100000	H' FF	H' 10	KEY CODE
2	10100000	H' FF	H' 09	xxxx101
3	10101010	H' 00	H' 00	WRITE DATA

FIG.10

SERIAL EEPROM

TOKYO ELECTRON LTD.

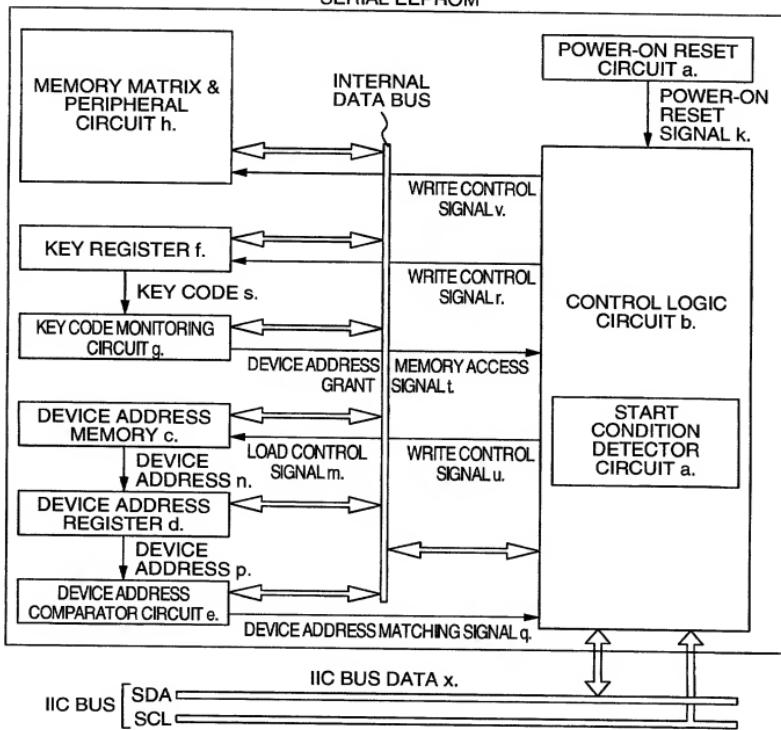


FIG. 11

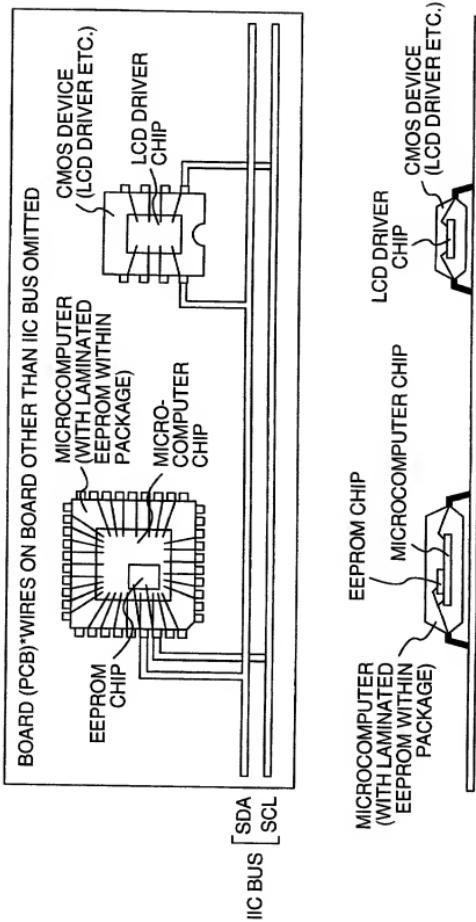


FIG. 12

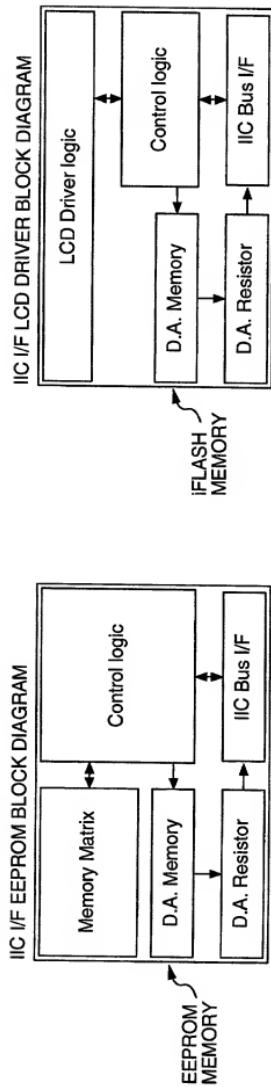
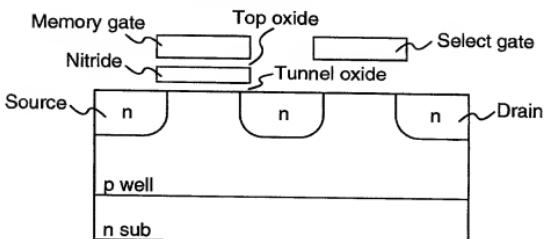
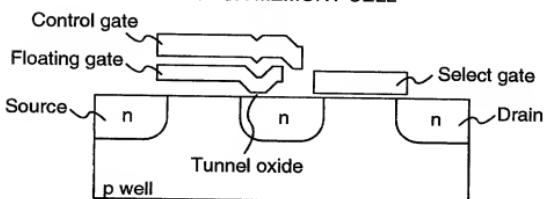


FIG. 13
MONOS MEMORY CELL



FLOTOX MEMORY CELL



iFLASH MEMORY CELL

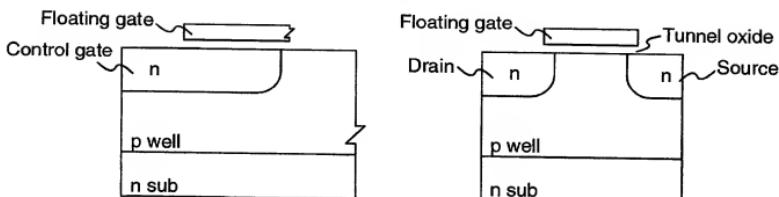
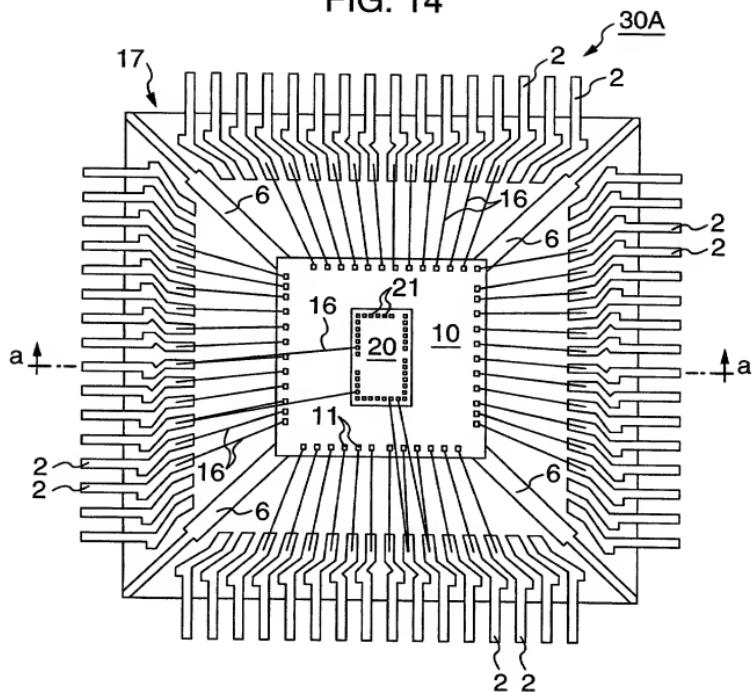


FIG. 14



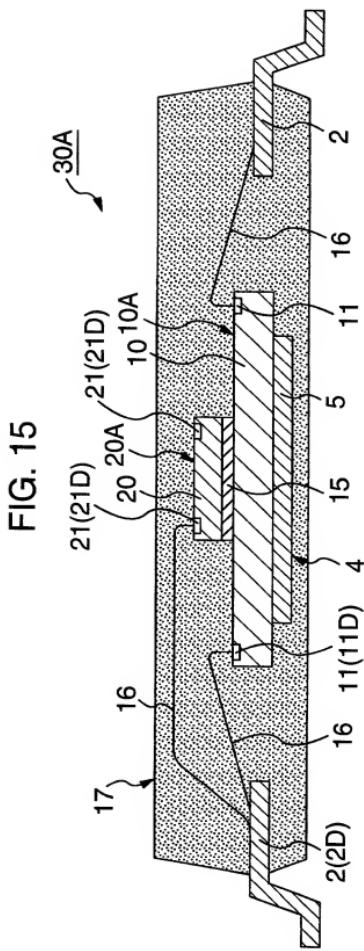


FIG. 16

<MICROCOMPUTER>

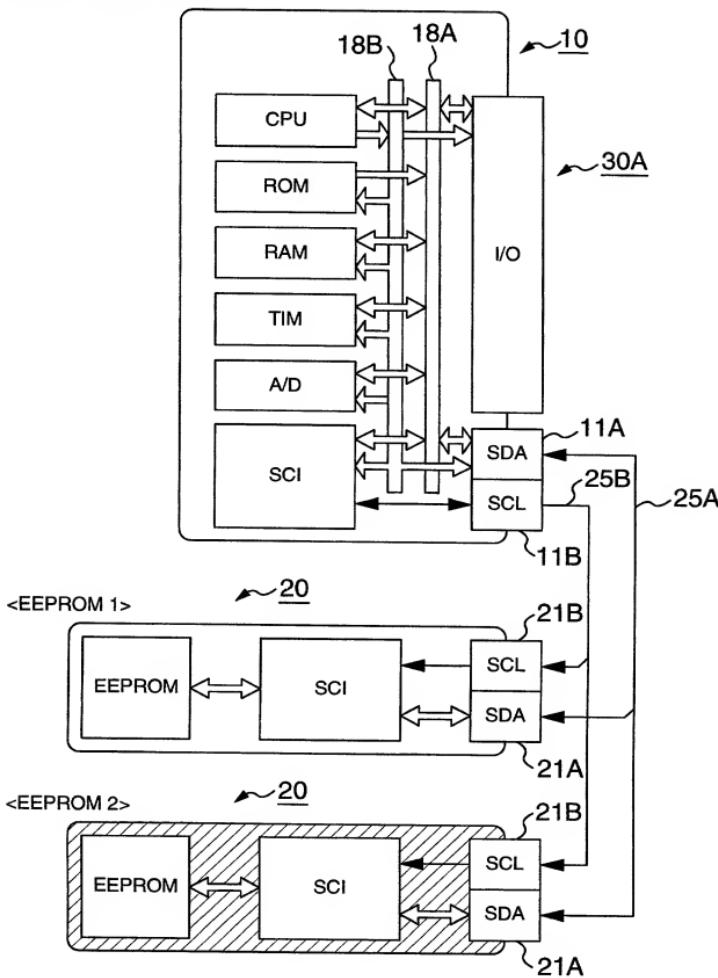


FIG. 17

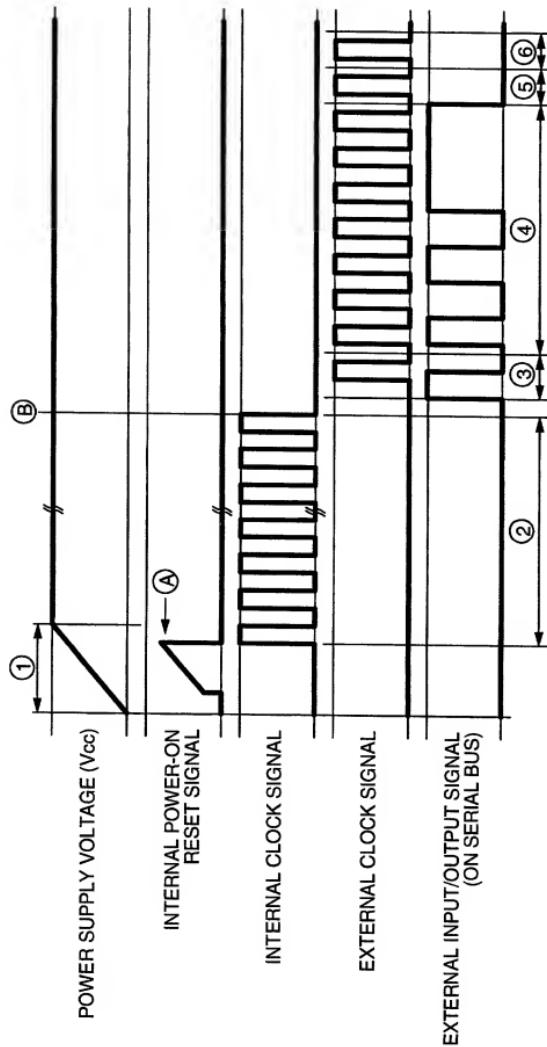


FIG. 18

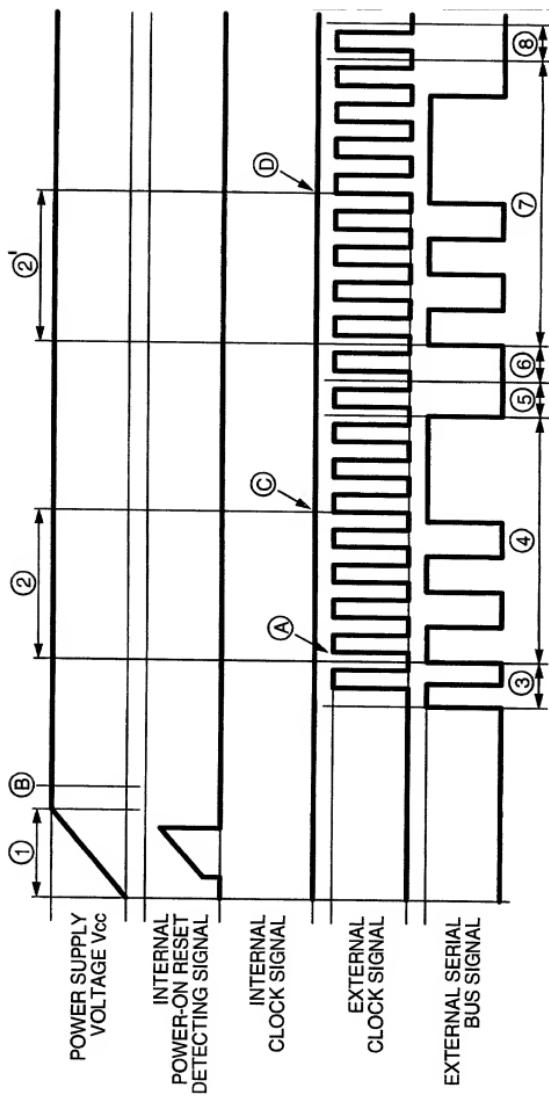


FIG. 19

